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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
08/993,442	12/18/1997	EARLE W. JENNINGS III	939A-040310	5108
7590 03/12/2004			EXAMINER	
ROBERT C COLWELL			NGO, CHUONG D	
TOWNSEND AND TOWNSEND AND CREW TWO EMBARCADERO CENTER 8TH FLOOR SAN FRANCISCO, CA 94111			ART UNIT	PAPER NUMBER
			2124	26
			DATE MAILED: 03/12/2004	38

Please find below and/or attached an Office communication concerning this application or proceeding.

				PREJ			
-		Application t	Applicant(s)				
	• • • • • • • • • • • • • • • • • • •	08/993,442	JENNINGS, EARLI	EW.			
	Office Action Summary	Examiner	Art Unit				
		Chuong D Ngo	2124				
Period fo	The MAILING DATE of this communication ap or Reply	opears on the cover sheet v	vith the correspondence add	dress			
THE - Exte after - If the - If NO - Failu Any	MORTENED STATUTORY PERIOD FOR REP MAILING DATE OF THIS COMMUNICATION ansions of time may be available under the provisions of 37 CFR 1 rs IX (6) MONTHS from the mailing date of this communication. The period for reply specified above is less than thirty (30) days, a repoperiod for reply is specified above, the maximum statutory period to reply within the set or extended period for reply will, by staturely received by the Office later than three months after the mailined patent term adjustment. See 37 CFR 1.704(b).	I.  1.136(a). In no event, however, may a eply within the statutory minimum of th d will apply and will expire SIX (6) MC tte, cause the application to become A	a reply be timely filed irty (30) days will be considered timely INTHS from the mailing date of this con ABANDONED (35 U.S.C. § 133).	: mmunication.			
Status							
1)⊠	Responsive to communication(s) filed on 11	February 2004.					
· · · · · · · · · · · · · · · · · · ·		is action is non-final.					
3)[	tters, prosecution as to the	merits is					
	closed in accordance with the practice under	Ex parte Quayle, 1935 C.	D. 11, 453 O.G. 213.				
Disposit	ion of Claims						
4)⊠	Claim(s) 20,23,25-28 and 30-35 is/are pendir	ng in the application.					
	4a) Of the above claim(s) is/are withdr	awn from consideration.					
5)⊠	Claim(s) <u>20</u> is/are allowed.						
6)⊠	Claim(s) <u>23,25-28 and 30-35</u> is/are rejected.						
7)	Claim(s) is/are objected to.						
8)[	Claim(s) are subject to restriction and/or election requirement.						
Applicat	ion Papers						
9)[	The specification is objected to by the Examir	ner.					
10)[	The drawing(s) filed on is/are: a) ac	cepted or b) objected to	by the Examiner.				
	Applicant may not request that any objection to th	e drawing(s) be held in abeya	ance. See 37 CFR 1.85(a).				
	Replacement drawing sheet(s) including the corre	ction is required if the drawin	g(s) is objected to. See 37 CF	R 1.121(d).			
11)	The oath or declaration is objected to by the B	Examiner. Note the attache	ed Office Action or form PT	O-152.			
Priority (	under 35 U.S.C. § 119						
	Acknowledgment is made of a claim for foreign All b) Some * c) None of:  1. Certified copies of the priority document Certified copies of the priority document Copies of the certified copies of the priority document Copies of the certified copies of the principle application from the International Bure	nts have been received. nts have been received in a iority documents have bee	Application No	Stage			
* (	See the attached detailed Office action for a lis	, ,,,	t received.	·			
A440b	24/2)						
Attachmen	n(s) ce of References Cited (PTO-892)	4) 🗀 Intonúa	Summon (PTO 442)				
	ce of References Cited (PTO-892) ce of Draftsperson's Patent Drawing Review (PTO-948)		Summary (PTO-413) o(s)/Mail Date				
3) 🔲 Infon	mation Disclosure Statement(s) (PTO-1449 or PTO/SB/06 er No(s)/Mail Date		Informal Patent Application (PTO	-152)			

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## **DETAILED ACTION**

1. Claims 23,25-28 and 30-35 are rejected under 35 U.S.C. 102(b) as being by Yamauchi et al. "Architecture and Implementation of a Highly Parallel Single-Chip Video DSP".

Yamauchi et al. also disclose in figure 6 an integrated circuit having a plurality of processing circuits (IDSP) coupled by communication ports (PIO). Yamauchi et al. also discloses in figure 2 the processing circuit has an interfacing circuit (PIO0-2) configured to control access to a memory (see page 209, col. 2, lines 15-26), an embedded processor (PROG.SEQ), and an array processor having a first through fourth MAC units (DPU0-3). Each MAC unit (DPUi) is coupled to a local memory (CMi) (see page 209, col. 2, lines 1-7), a shared operand unit (WM or IN1) for simultaneously providing a shared operand to the MAC units via a share bus (VBUS8~9), and a share output and feedback interface (VBUS4~7) as claimed.

- 1. Claim 20 is allowed.
- 2. Applicant's arguments filed on 02-11-04 have been fully considered but they are not persuasive with respect to claims 23,25,26-28 and 30-35 since Yamauchi et al., as explained in the rejection, does provide the features that applicant argued.

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3. The text of those sections of Title 35, U.S. Code not included in this action can be

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found in a prior Office action.

4. Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Chuong D Ngo whose telephone number is (703) 305-9764.

The examiner can normally be reached on Tuesday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Kakali Chaki can be reached on (703) 309-9662. The fax phone number for the

organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent

Application Information Retrieval (PAIR) system. Status information for published

applications may be obtained from either Private PAIR or Public PAIR. Status information for

unpublished applications is available through Private PAIR only. For more information about

the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the

Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-

free).

Chuong D Ngo Primary Examiner

Oley

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